REMARKS

Claims 1, 2 and 4-14 and 16-24 are pending in the application.

Claims 9, 14, 16-24 have been cancelled herein.

Claims 1, 2, 4-8, 9-13 remain pending.

Claims 10-13 have been amended to depend from claim 1.

Claim 2 is found to contain allowable subject matter. The Examiner listed no prior art rejection with regard to claim 1 however the Examiner does not list claim 1 as allowable.

The pending claims have been amended to clarify applicant's claimed invention. No new matter is entered since the claims are clarified in accordance with the original disclosure.

Claims 1, 2, 4-14 and 16-24 are rejected under 35 U.S.C.§ 112, second paragraph, as being indefinite.

The claims have been clarified as mention above, therefore it is respectfully requested the rejection be withdrawn.

Prior Art Rejections

Claim 9 is rejected under 35 U.S.C.§102(e) as anticipated by the article of Robertson. Robertson was previously used in rejecting claim 1. Claim 9 is cancelled obviating the rejection.

Claim 1

Applicant's claim 1 recites a turbo decoder for iteratively decoding received signals up to a set number of times which includes a controller which, when absence of error has been detected, in results of the first decoding processing, is operable for outputting the results of the first decoding processing and halting the decoding operation of the second decoding processing even if the number of times decoding has been performed has not attained said set number of times.

Robertson fails to teach at least this feature of applicant's claimed invention.

It is admitted in the Office Action that Robertson provides no suggestion for stopping decoding after a fixed number of iterations. It is respectfully submitted that Robertson fails to suggest applicant's features and in addition does not suggest the combination of features claimed.

It is respectfully submitted that claim 1 should be allowed.

Claims 4, 11, 13-14 and 16-24 are rejected under 35 U.S.C.§102(e) as being anticipated by Chennakeshu et al. (US 6,192,503) (hereinafter Chennakeshu). Claims 14, 16-24 have been cancelled obviating the rejection. Claim 11 now depends from claim 1 and the rejection should be withdrawn.

Claim 4

Applicant's claim 4 includes a combination of features which are not suggested by the Chennakeshu reference. Claim 4 includes that: in order to render an error pattern in decoded bursty data, results of final decoding processing are output from said second elementary decoder directly without intervention of interleaving or deinterleaving.

Chennakeshu teaches a decoder determines which of the first and second decoding means will first generate an estimate of a symbol in the source sequence based upon the size of the received signals ya and yb. For example Fig. 9 illustrates operations for decoding first and second received sequences wherein decoding is guided by a determination of a signal characteristic for each of the received sequences. A received sequence having the greater signal strength is first decoded according to its corresponding error correction code to produce a first estimate of a symbol in the source sequence. If the first estimate satisfies a predetermined reliability criterion, the estimate may be output.

If not, a second one of the received sequences is decoded according to its corresponding error correction code augmented by the first estimate or, alternatively, a predetermined reference value, to produce a new estimate of the symbol. As with the first estimate, if the new estimate satisfies the predetermined reliability criterion, it may be output. If not, this estimate is used to generate a new estimate of the symbol from the first one of the received sequences, the reliability of which is in turn tested to determine if further decoding is necessary.

The decoder of Chennakeshu fails to teach the features of claim 4 to render an error pattern in decoded bursty data, results of final decoding processing are output from said second elementary decoder directly without intervention of interleaving or deinterleaving.

For at least the foregoing, it is respectfully submitted that the turbo decoder of claim 4 is not anticipated by Chennakeshu and is thus claim 4 is allowable.

Claims 5 and 8

Claims 5 and 8 are rejected under 35 U.S.C.§102(e) as anticipated by Pyndiah et al. (US 6,122,763).

In the Office Action it is argued that Pyndiah shows a turbo decoder in Fig. 6. It is submitted that Pyndiah may only show first and second decoding processing without showing or by a turbo decoder.

Applicant's claim 5 recites a turbo decoder ... and executing decoding processing repeatedly using these received signals including a selection circuit for selecting the signal yc when the first decoding processing is executed, selecting the signal yb when the second decoding processing is executed, and inputting the selected signal to the elementary decoder; and means for deinterleaving results of the first decoding processing, interleaving results of the second decoding processing and inputting the deinterleaved and interleaved results to the elementary

decoder; wherein results of decoding are output from said elementary decoder directly without intervention of interleaving or deinterleaving

Although a decoder of Pyndiah executes first and second decoding processing, Pyndiah fails to teach the decoding of turbo encoded data.

Additionally Pyndiah fails to teach a decoder that can render an error pattern bursty and cannot render an error pattern bursty or random selectively. Accordingly it is respectfully submitted that claims 5 and 8 are allowable.

Claims 6 and 7

Claims 6 and 7 are rejected under 103(a) as unpatentable over Chennakeshu. Official notice is taken of the advantages of limiting the number of iterations in a turbo code decoder and that it is well known with regard to the Smith reference. It is respectfully submitted that Smith should then be cited in this rejection.

Claims 6 and 7 include a similar feature of a selection circuit for selecting and outputting the results of first and second decoding processing output from said first and second elementary decoders based upon which of a bursty error pattern and a random error pattern is requested in decoded data.

Chennakeshu, Fig. 8 discloses a decoder that estimates first and second decoding result every time they are acquired and outputs a reliable decoding result when it is acquired. However it is respectfully submitted that Chennakeshu fails to show the selection circuit and being based upon which of a bursty error pattern and a random error pattern is requested in the decoded data.

Claims 6 and 7 realize a turbo decoder for rendering an error pattern bursty or random selectively and the turbo decoder is realized by the first to third selection circuits. Chennakeshu

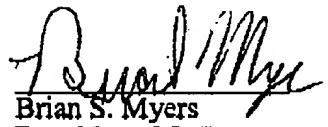
fails to teach or suggest these features and does not disclose these selection circuits. For at least the foregoing reasons it is respectfully submitted claims 6 and 7 are allowable.

Claim 10 is rejected under 35 U.S.C.§102(e) as anticipated by Sindhushayana et al. (U.S. 6,292,918). Claims 10-13 are amended to depend upon claim 1. This rejection of claim 10 should be withdrawn.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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